Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A method for generating at least one instruction for execution by a central processing unit, the method comprising the steps of:

receiving a misaligned instruction address;

causing an exception in response to said misaligned instruction address; and

executing, in response to said exception, an exception handling routine~~, said routine~~ that includes the steps of

transforming data into at least one instruction for execution by the central processing unit,

storing said at least one instruction into memory at a first address,

loading said first address into a program counter register of said central processing unit, and

returning from execution of said exception handling routine to execute said at least one instruction stored at said first address.

2. (canceled)

3. (currently amended) The method of claim 1, wherein said executing step comprises the step of:

~~transforming~~ using said misaligned instruction address ~~into~~ to form said at least one instruction.

4. (currently amended) The method of ~~claim 2~~ claim 1, wherein said executing step further comprises a step prior to said returning step of:

performing the operations necessary to clear an exception flag and put said central processing unit into its previous execution mode.

5. (previously presented) The method of claim 1, wherein said executing step further comprises:

transforming said misaligned instruction address into an address where data is stored.

6. (currently amended) The method of claim 1, wherein said transforming data step is selected from the group consisting of: decompressing a compressed instruction, decrypting an encrypted instruction, decoding a macro ~~instruction;~~ instruction, and transforming a non-native instruction into said at least one instruction ~~and causing a random number of processor instructions to be performed~~.

7. (original) The method of claim 5, wherein said transforming said misaligned instruction address step is selected from the group consisting of: using the misaligned instruction address, adding an offset to the misaligned instruction address and using a lookup table.

8. (currently amended) A computer readable medium having digital information stored thereon, the digital information defining executable computer program logic, wherein the executable computer program ~~logic~~ logic, when executed, causes a processor to perform the steps of: ~~performs the following steps:~~

receiving a misaligned instruction address;

generating an exception; and

executing, in response to said exception, an exception handling routine~~, said routine~~ that includes the steps of

transforming data into at least one instruction,

storing said at least one instruction into memory at a first address,

loading said first address into a program counter register of said central processing unit, and

returning from execution of said exception handling routine to execute said at least one instruction stored at said first address.

9. (canceled)

10. (currently amended) The computer readable medium of claim 8, wherein said executing step comprises the step of:

~~transforming~~ using said misaligned instruction address ~~into~~ to form said at least one instruction.

11. (currently amended) The computer readable medium of ~~claim 9~~ claim 8, wherein said executing step further comprises a step prior to said returning step of:

performing the operations necessary to clear an exception flag and put said central processing unit into its previous execution mode.

12. (currently amended) The computer readable medium of ~~claim 9~~ claim 8, wherein said executing step further comprises:

transforming said misaligned instruction address into an address where data is stored.

13. (currently amended) The computer readable medium of claim 8, wherein said transforming data step is selected from the group consisting of: decompressing a compressed instruction, decrypting an encrypted instruction, decoding a macro ~~instruction;~~ instruction, and transforming a non-native instruction into said at least one instruction ~~and causing a random number of processor instructions to be executed~~.

14. (original) The computer readable medium of claim 12, wherein said transforming said misaligned instruction address step is selected from the group consisting of: using the misaligned instruction address, adding an offset to the misaligned instruction address, and using a lookup table.

15. (currently amended) An apparatus for generating valid processor instructions, comprising:

~~first~~ means for receiving a misaligned instruction address;

~~second~~ means for generating an exception in response to said misaligned instruction address; ~~and~~

~~third~~ means for transforming data into at least one instruction in response to said exception;

means for storing said at least one instruction into memory at a first address;

means for loading said first address into a program counter register of said central processing unit; and

means for returning from execution of an exception handling routine to execute said at least one instruction stored at said first address.

16. (canceled)

17. (canceled)

18. (currently amended) The apparatus of claim 15, wherein said ~~third~~ transforming data means comprises:

means for ~~transforming~~ using said misaligned instruction address ~~into~~ to form said at least one instruction.

19. (currently amended) The apparatus of claim 15, ~~where~~ wherein said ~~third~~ transforming data means comprises:

means for transforming said misaligned instruction address into a memory address and for using said memory address to fetch said at least one instruction from memory.

20. (currently amended) A computer system, comprising:

a processor;

a memory, coupled to said processor; and

sequences of instructions stored in said memory which, when executed ~~by said processor~~, cause said processor to:

~~receive a misaligned instruction address;~~

execute an exception handling routine in response to ~~said~~ a misaligned instruction address~~; and~~ that

~~transform~~ transforms data stored in said memory into ~~valid processor instructions~~ at least one instruction, ~~in response to said exception~~

stores said at least one instruction into said memory at a first address, loads said first address into a program counter register of said processor, and

returns from execution of said exception handling routine to execute said at least one instruction stored at said first address.

21. (new) The apparatus of claim 15, wherein said transforming data means decompresses a compressed instruction.

22. (new) The apparatus of claim 15, wherein said transforming data means decrypts an encrypted instruction.

23. (new) The apparatus of claim 15, wherein said transforming data means decodes a macro instruction.

24. (new) The apparatus of claim 15, wherein said transforming data means transforms a non-native instruction into said at least one instruction.

25. (new) The computer system of claim 20, wherein said data is transformed into at least one instruction by decompressing a compressed instruction.

26. (new) The computer system of claim 20, wherein said data is transformed into at least one instruction by decrypting an encrypted instruction.

27. (new) The computer system of claim 20, wherein said data is transformed into at least one instruction by decoding a macro instruction.

28. (new) The computer system of claim 20, wherein said data is transformed into at least one instruction by transforming a non-native instruction into said at least one instruction.